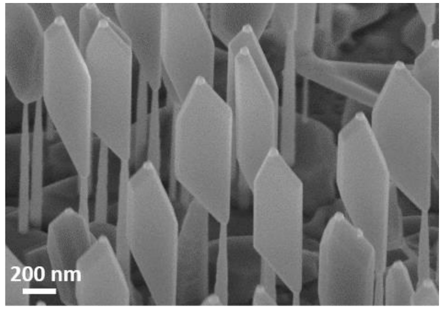
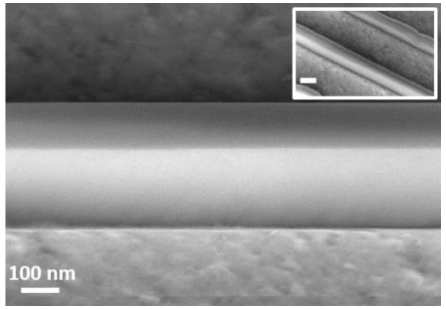


InSb nanostructures : Morphology control by tuning growth parameters

PhD. in Nanoscience (Second year)



Candidate:

Isha Verma

Supervisor:

Prof. Lucia Sorba

NEST

SCUOLA
NORMALE
SUPERIORE

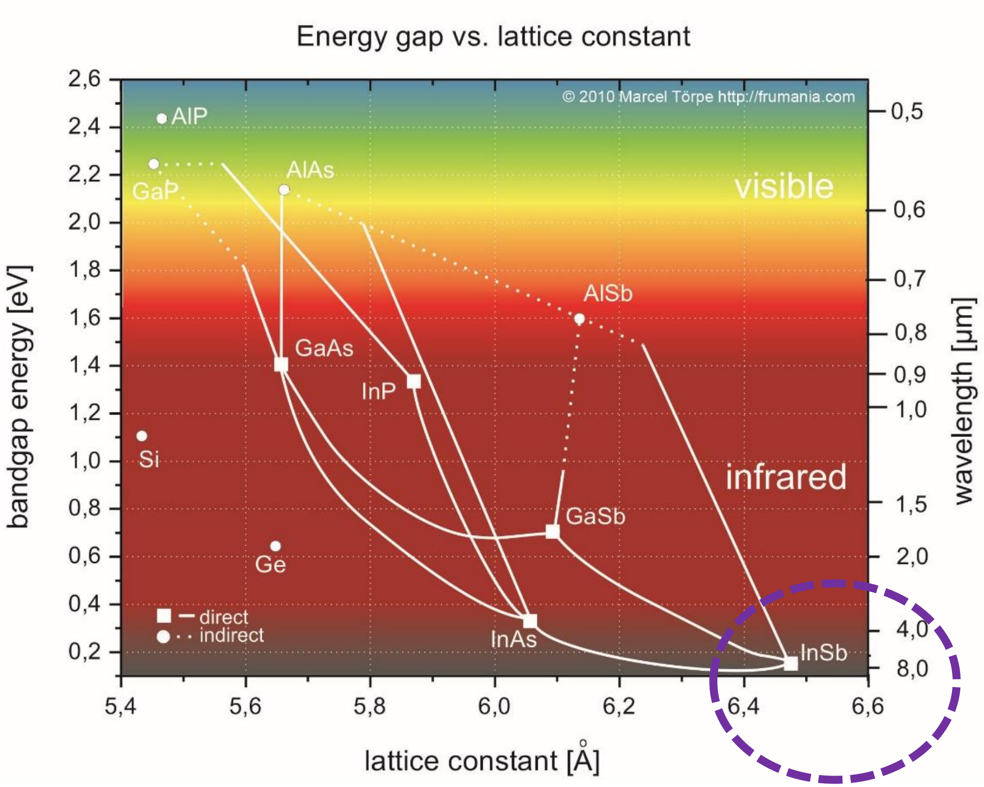
OUTLINE

- Introduction
- Motivation
- Growth Technique- Chemical Beam Epitaxy (CBE)
- Growth Approach I: Au assisted CBE
- Growth Approach II: Selective area epitaxy (SAE)
- Future plan

INTRODUCTION

Indium antimonide (InSb)

- Energy band gap $E_g = 0.17$ eV at 300K
- Low effective carrier mass
- High electron mobility
- Large Landé g factor



Perfect system for:

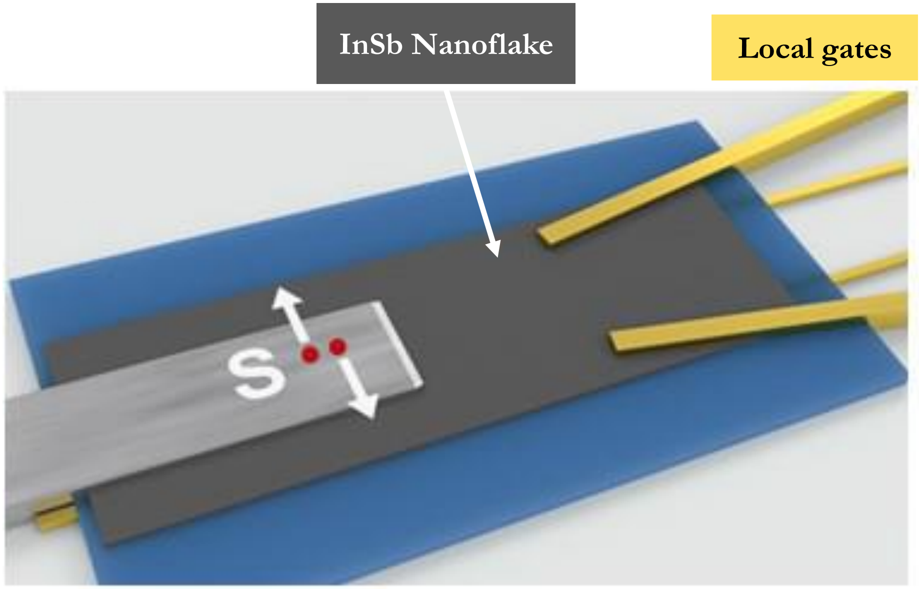
- Detection exotic bound states at the superconductor/semiconductor interface

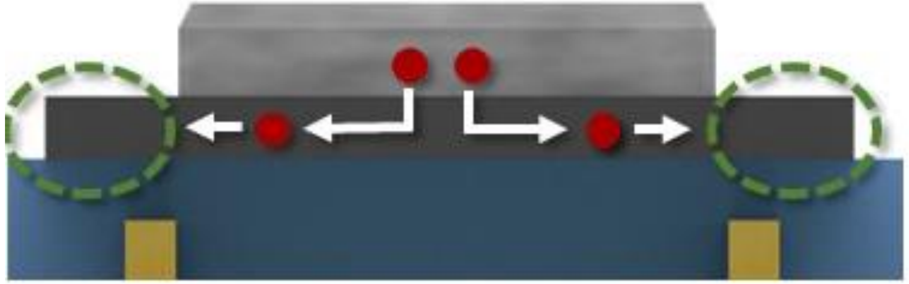
MOTIVATION

TOPOLOGICALLY PROTECTED STATES IN DOUBLE NW SUPERCONDUCTOR HYBRIDS

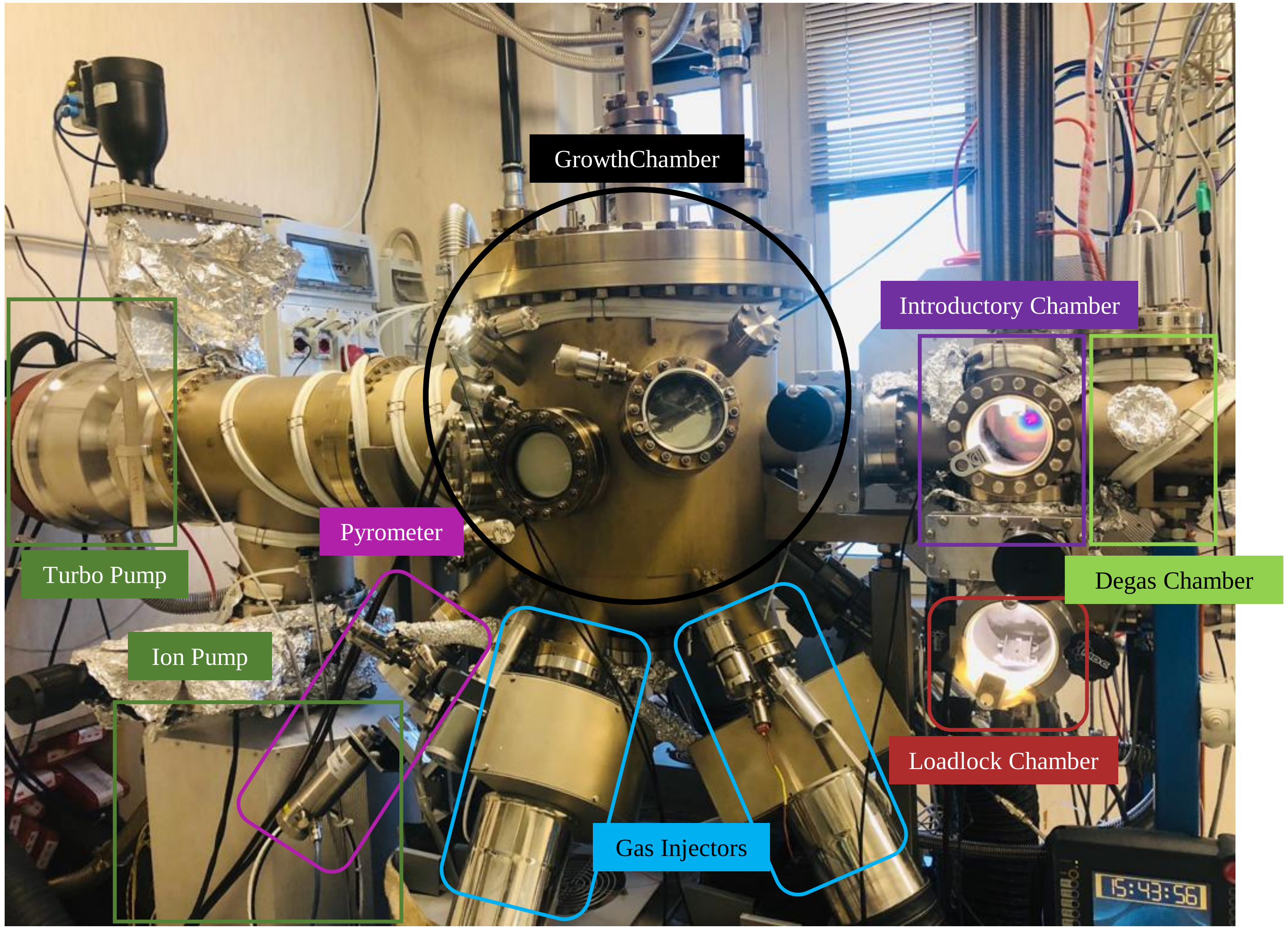
Double Nanowire device concept (DNW) based on InSb nanoflakes

InSb flake (dark gray) is deposited on thin local gates (yellow) covered by an insulator (blue). Local gates are used to confine 1D artificial nanowires (NW) electrostatically (see green region in lower cross-section panel). Placing a superconductor (S) between the NWs, superconducting proximity is induced in the middle segment of the flake (see lower panel), which serves as a S link between the NWs with small k_F.





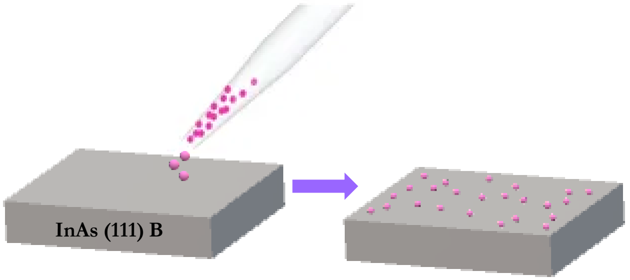
CHEMICAL BEAM EPITAXY (CBE)



- UHV (10^{-9} mbar)
- Epitaxial growth of nanostructures
- Metal organic gaseous precursors

GROWTH APPROACH I
AU ASSISTED CBE

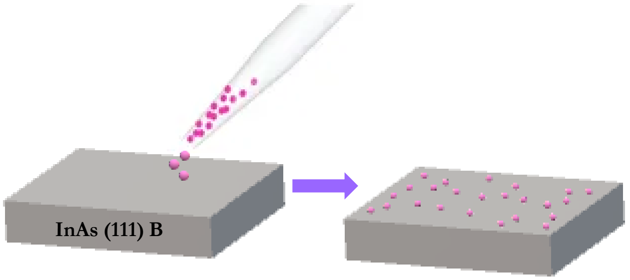
GROWTH APPROACH I: AU ASSISTED CBE



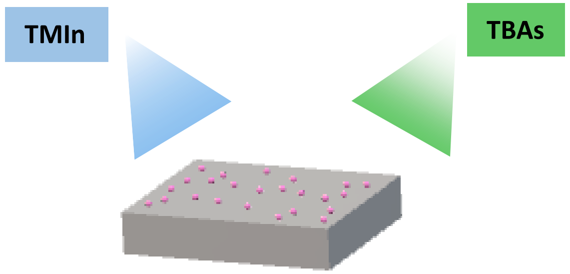
STEP 1

Drop-cast 30 nm Au colloids

Growth Approach I: Au assisted CBE

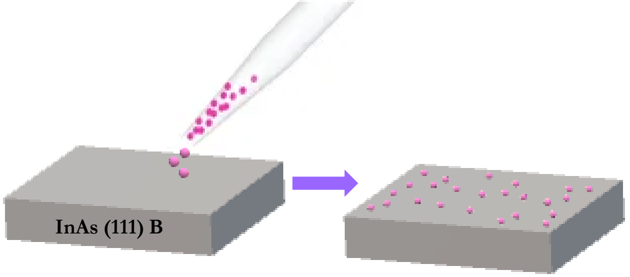


STEP 1
Drop-cast 30 nm Au colloids



STEP 2
Growth on InAs NWs

GROWTH APPROACH I: AU ASSISTED CBE



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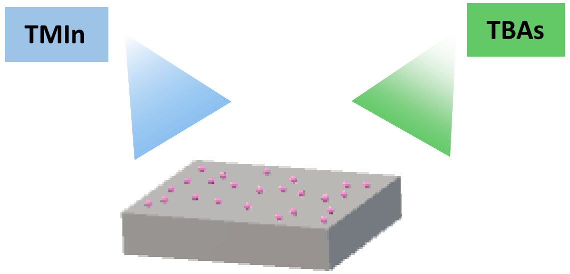
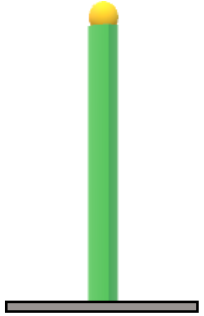


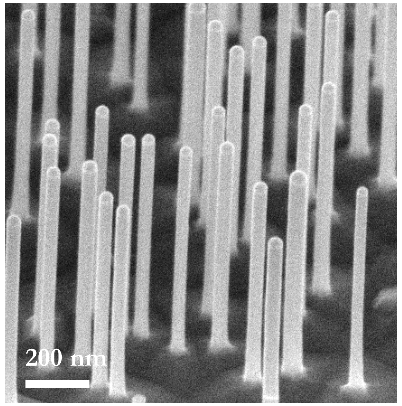
STEP 2
Growth on InAs NWs

TMIn: 0.6 Torr, TBAs: 1.5 Torr

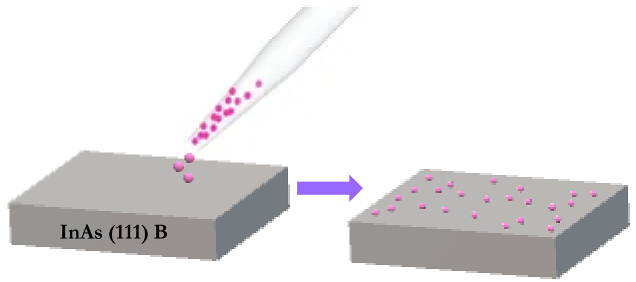
T_{InAs} = 385° ± 10° C

InAs NW





Growth Approach I: Au assisted CBE



STEP 1
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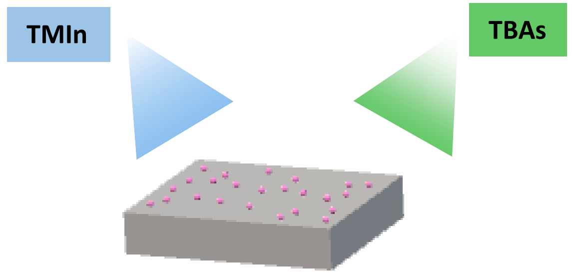

STEP 2
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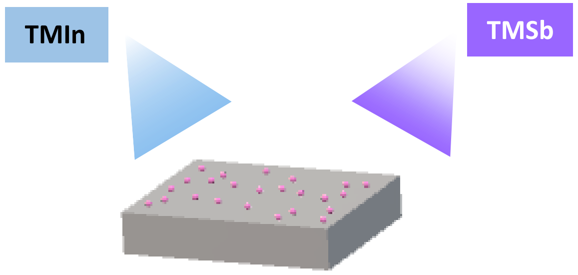
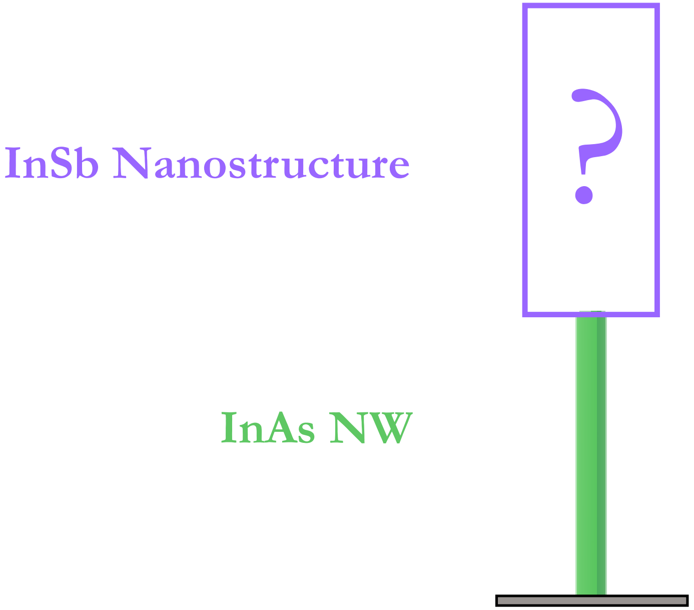
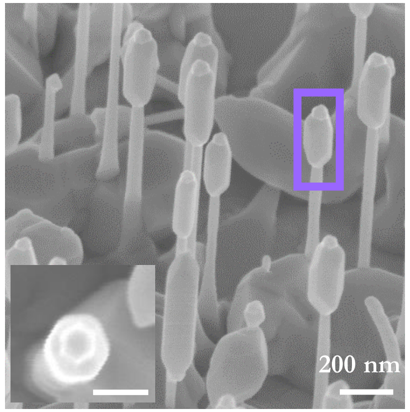


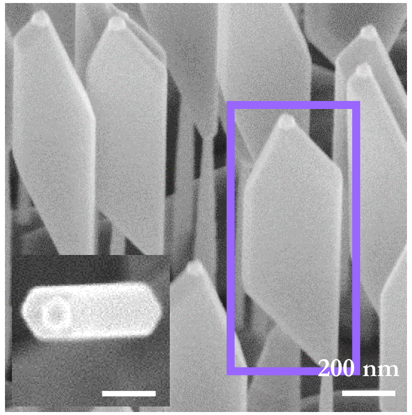
STEP 3
Growth on InSb nanostructures



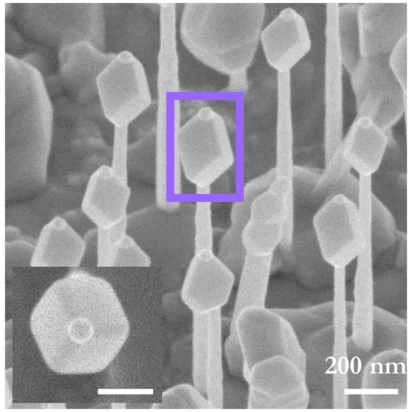
InSb Nanowires (1D)



InSb Nanoflags (2D)



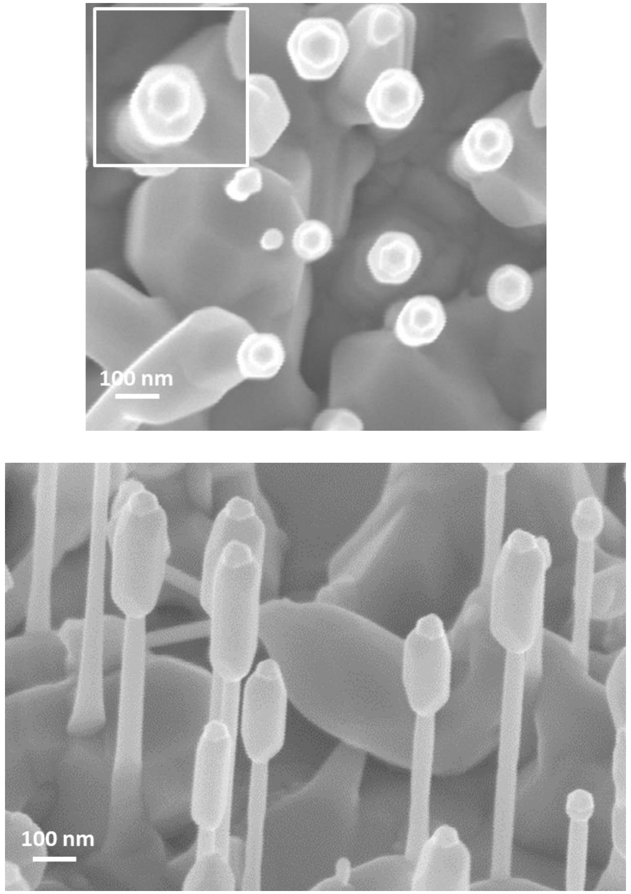
InSb Nanocubes (3D)



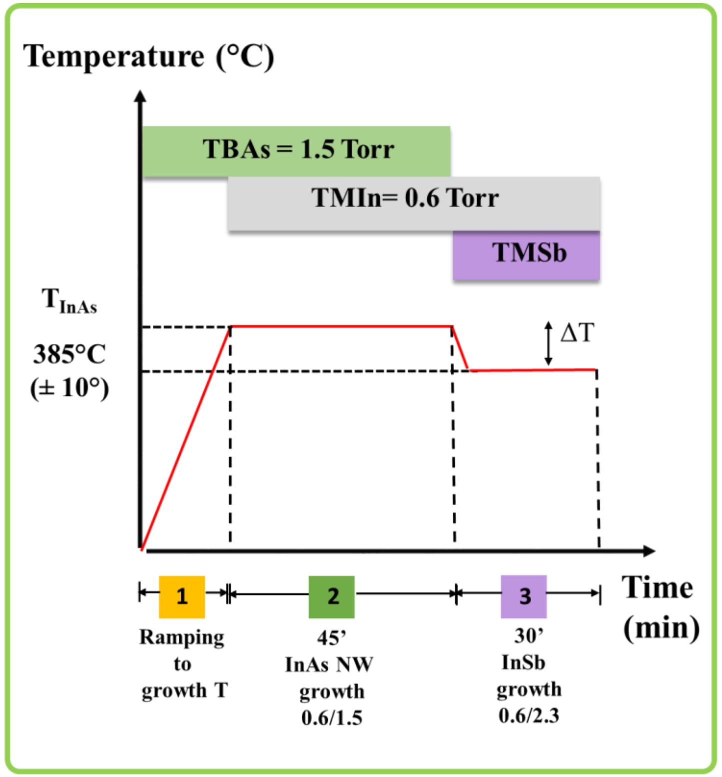
Morphological control by tunning growth parameters

Inset scale: 100 nm

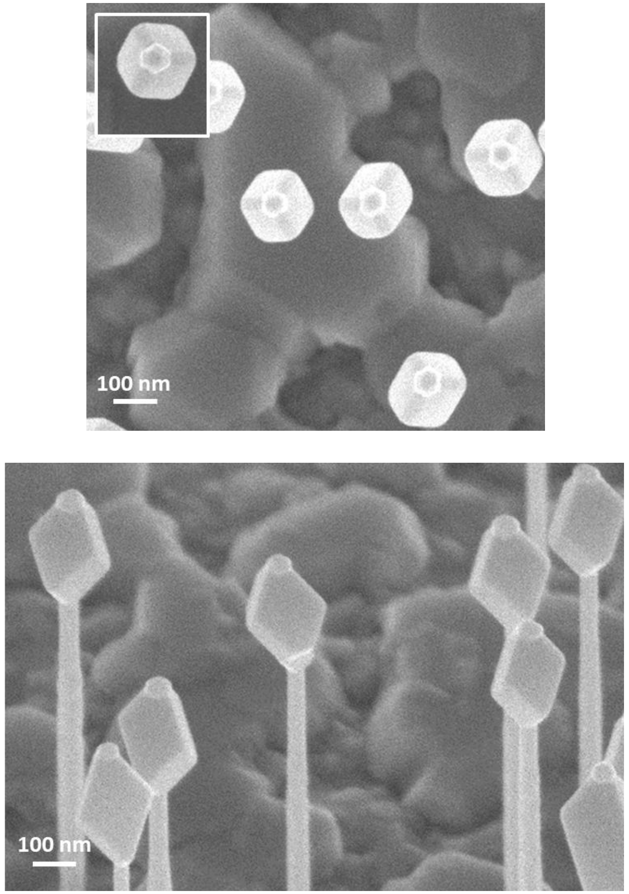
NANOWIRE TO NANOCUBES



ΔT= -30°C

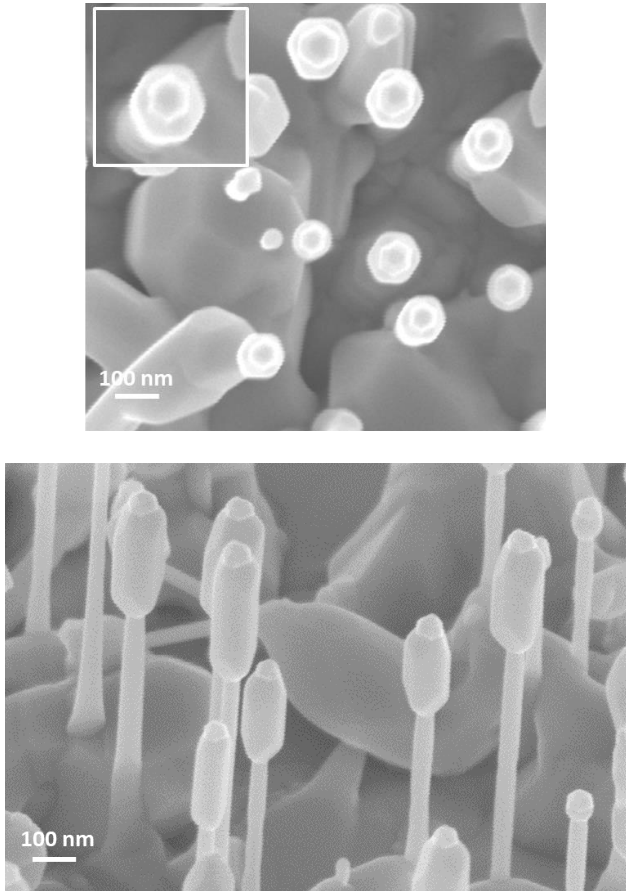


By changing the InSb temperature ΔT
NW → NC



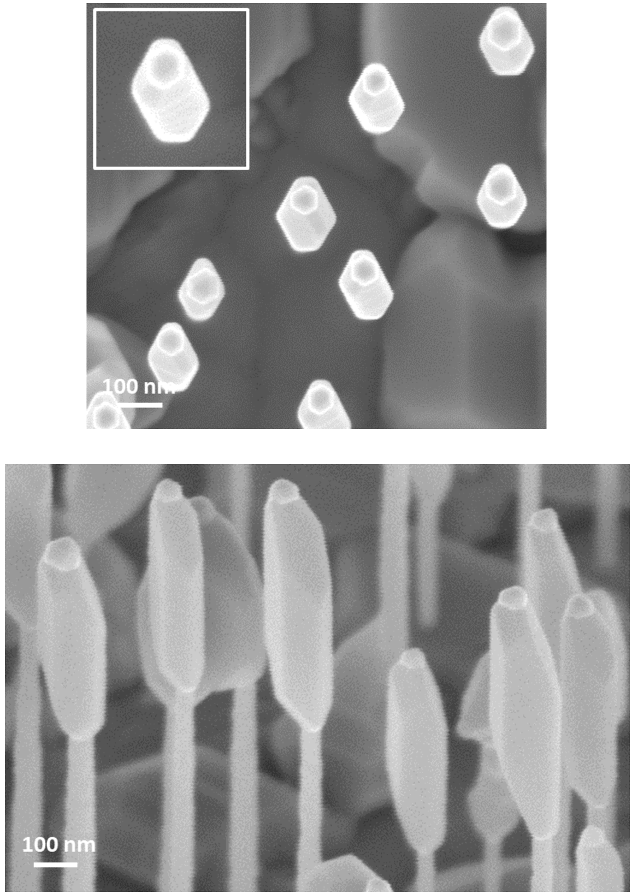
ΔT= -40°C

MORPHOLOGICAL CONTROL BY ROTATION

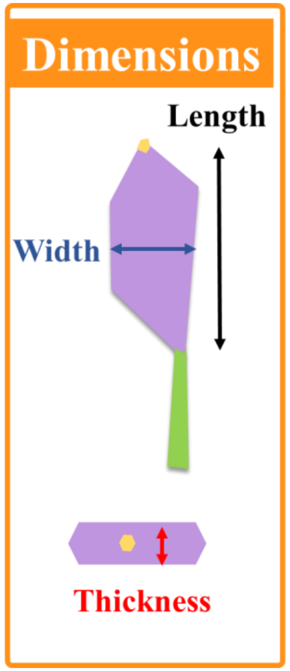


With Rotation

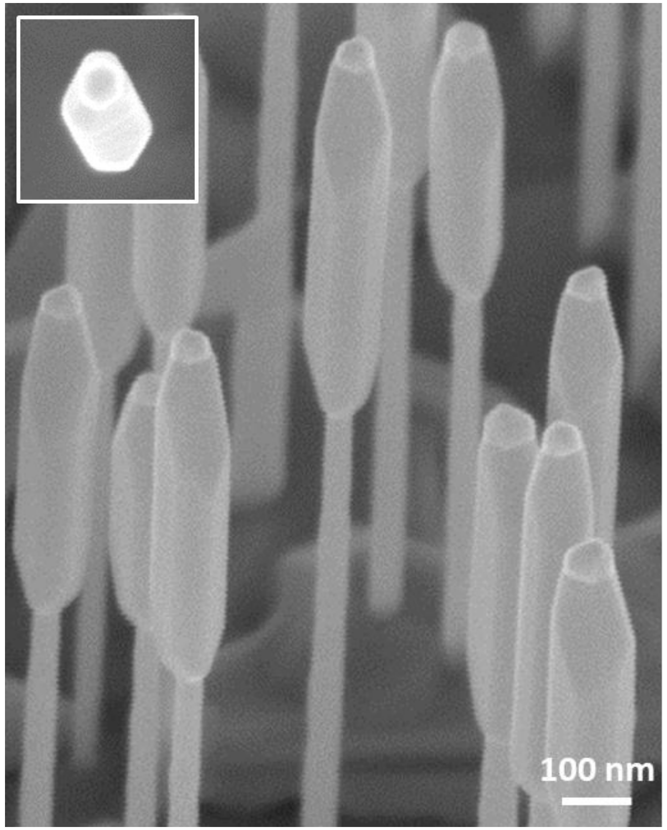
Asymmetry triggered by stopping rotation



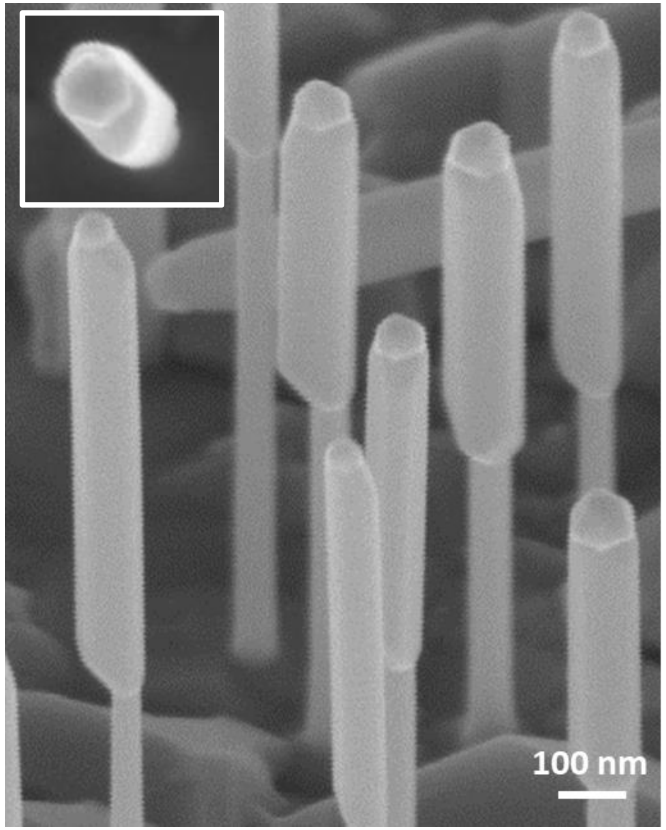
Without Rotation



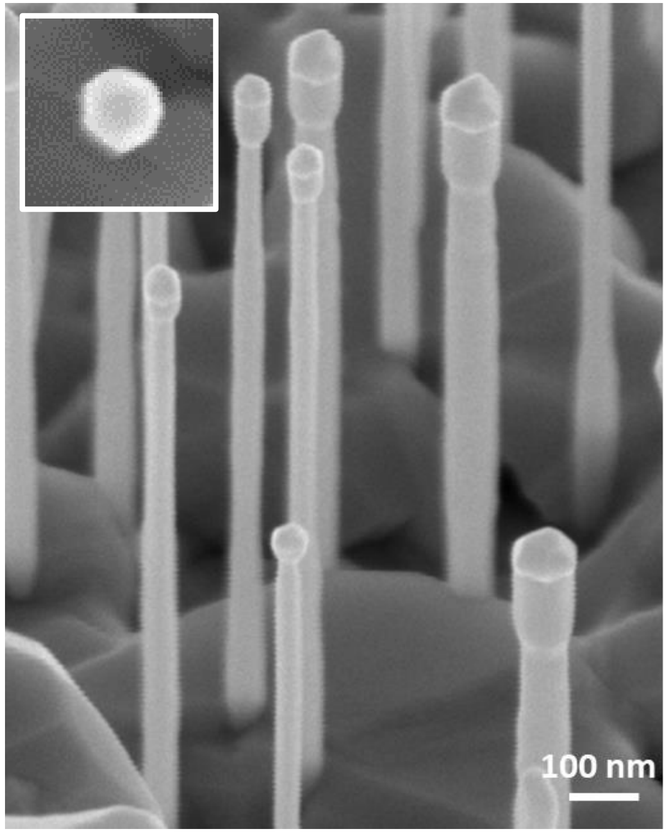
OPTIMIZING InSb TEMPERATURE



ΔT= -30°C



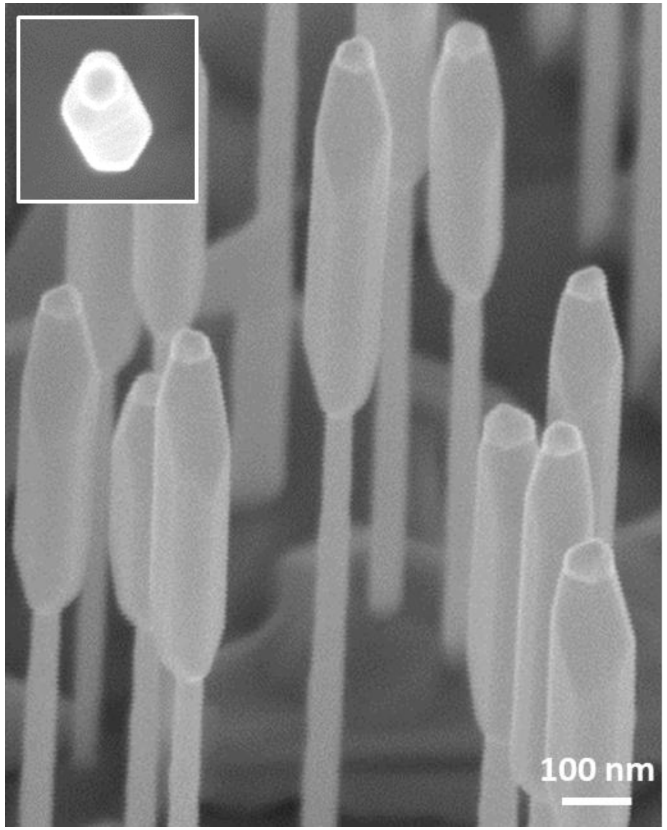
ΔT= -20°C



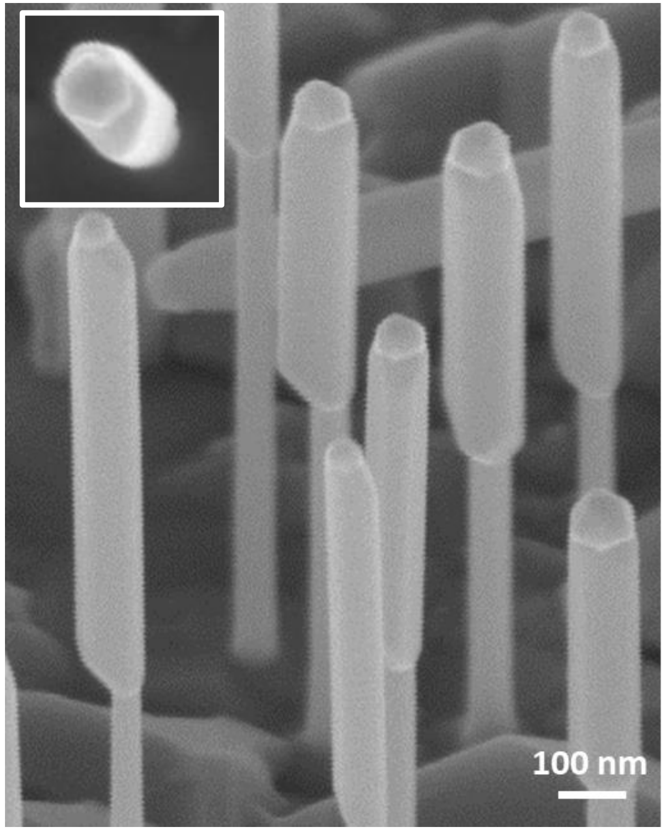
ΔT= -10°C

ΔT= -20°C is a good compromise

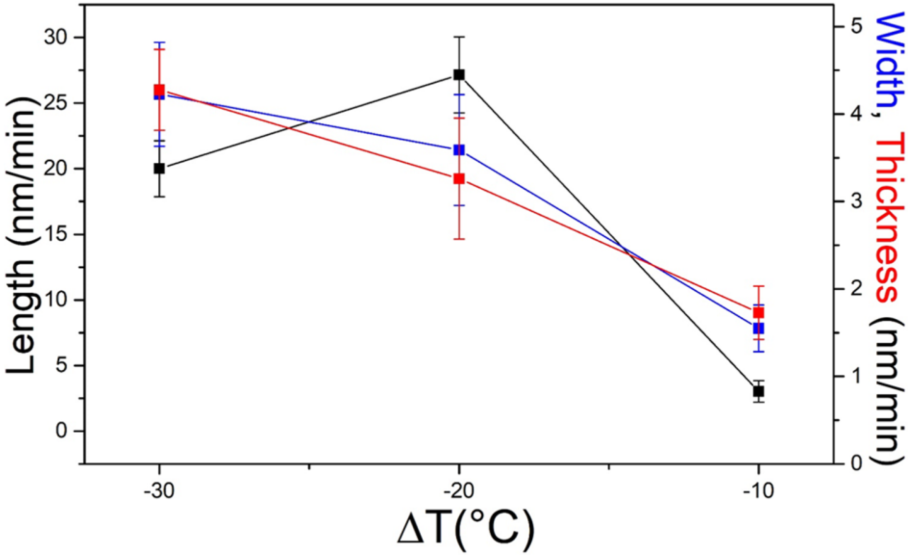
OPTIMIZING InSb TEMPERATURE



ΔT= -30°C

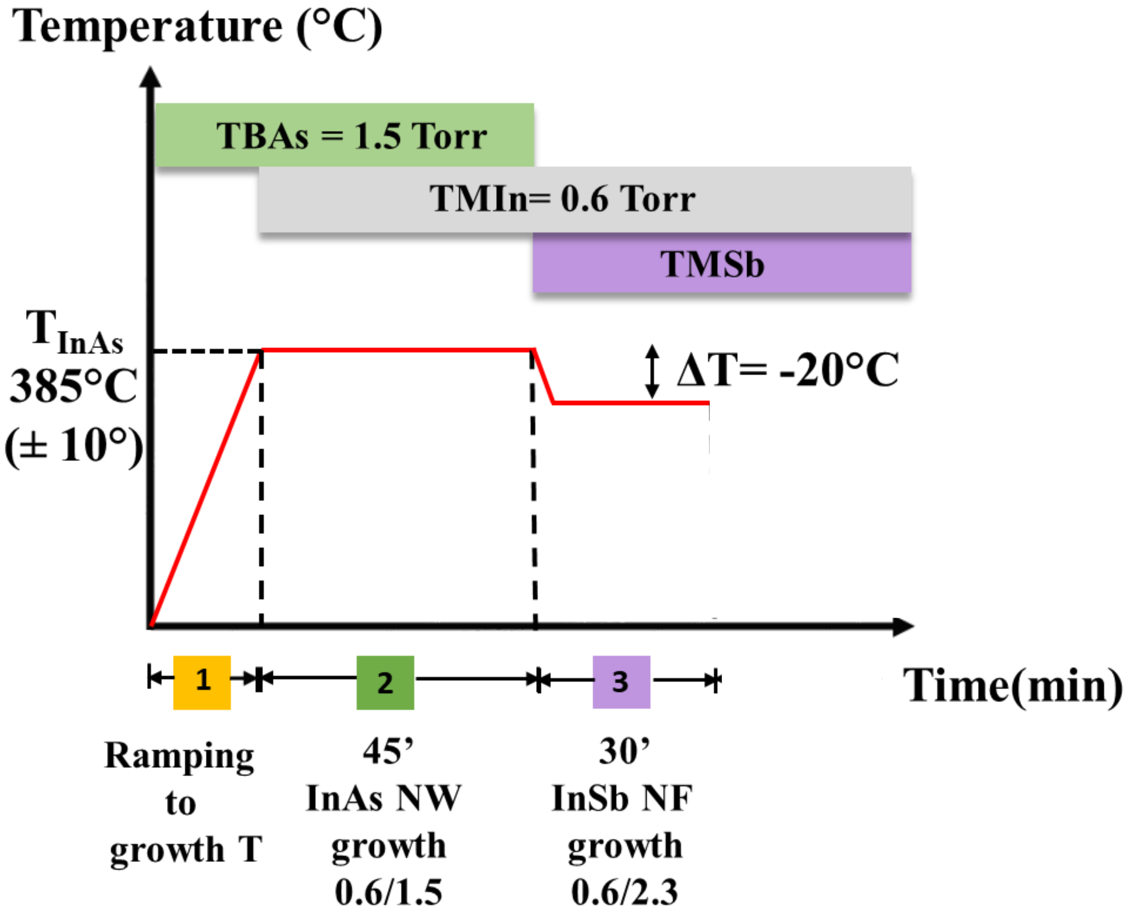


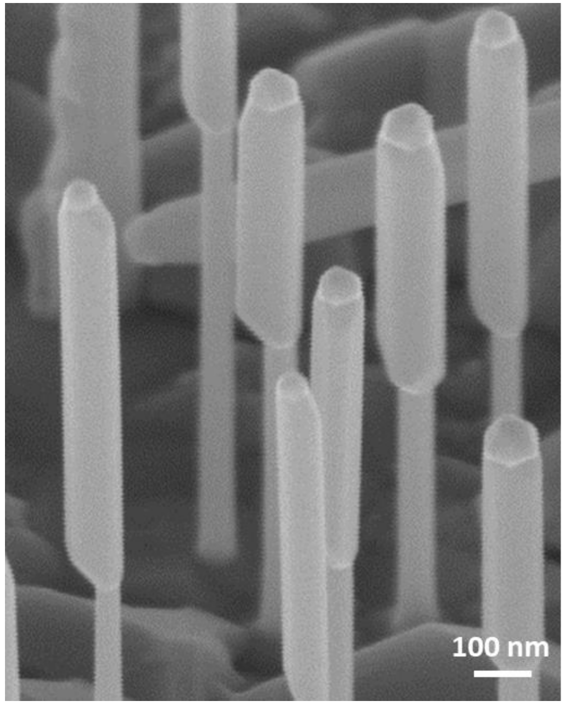
ΔT= -20°C



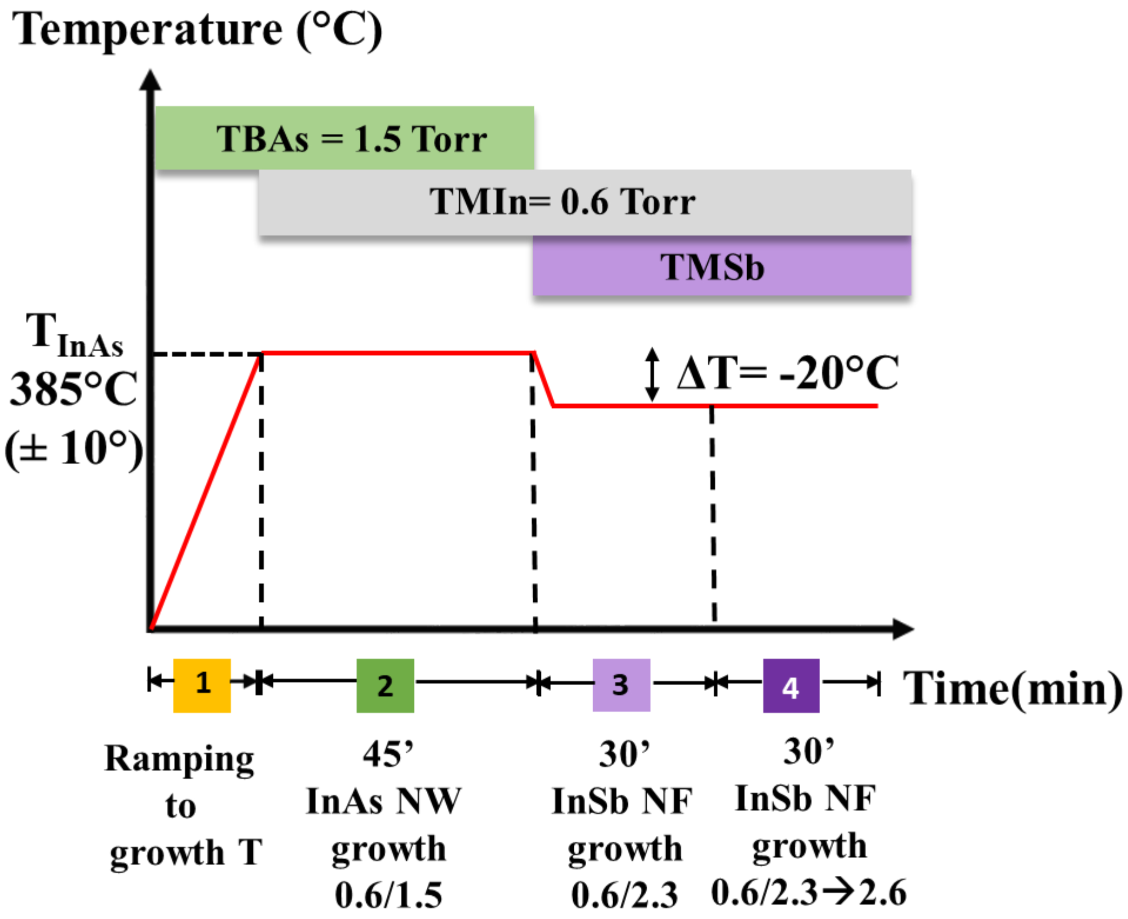
ΔT= -20°C is a good compromise

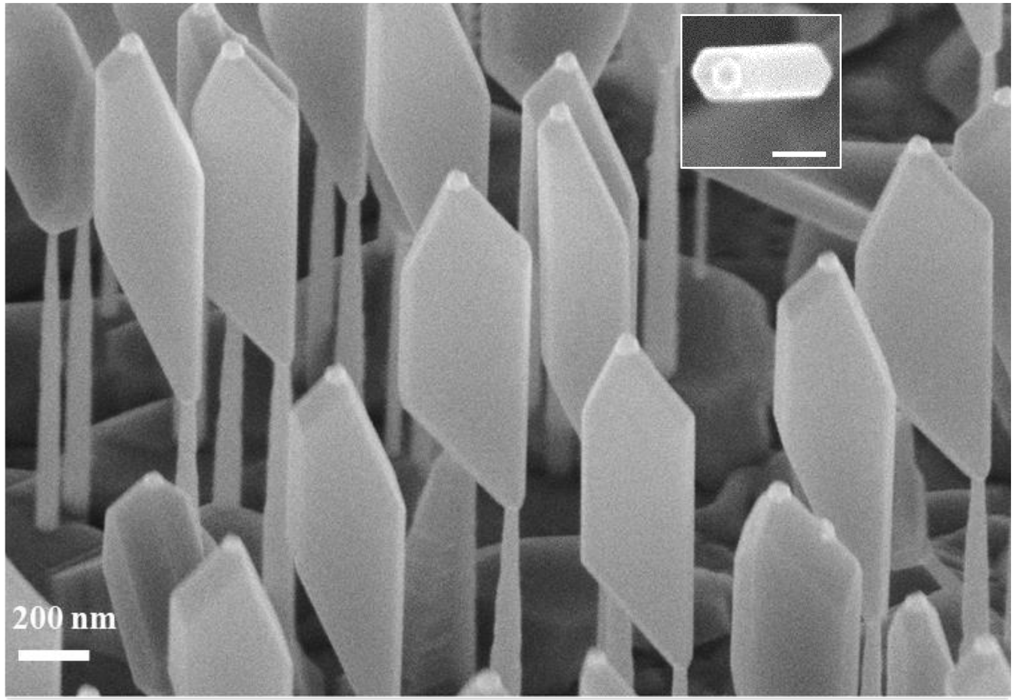
MORPHOLOGICAL CONTROL BY Sb FLUX





MORPHOLOGICAL CONTROL BY Sb FLUX



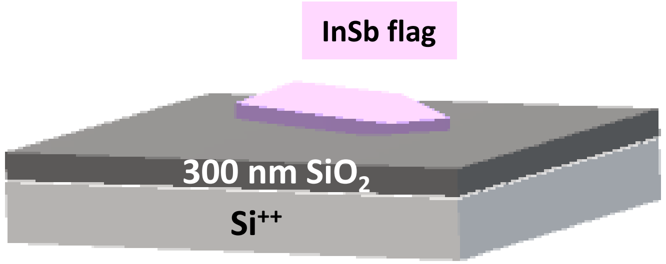


Length= (1.28 ± 0.14) µm

Width= (282.35 ± 86.48) nm

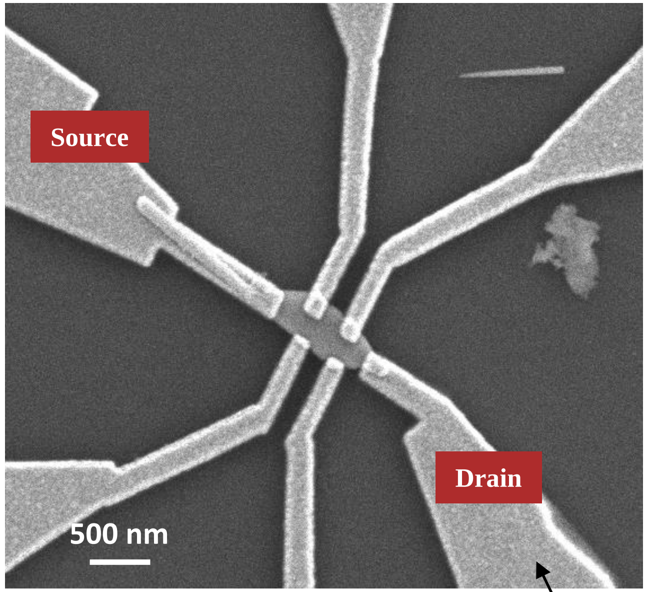
Thickness= (103.81 ± 17.18) nm

InSb NANOFLAGS: DEVICE FABRICATION AND TRANSPORT MEASUREMENTS



- InSb NFs are mechanically transferred to Si substrate

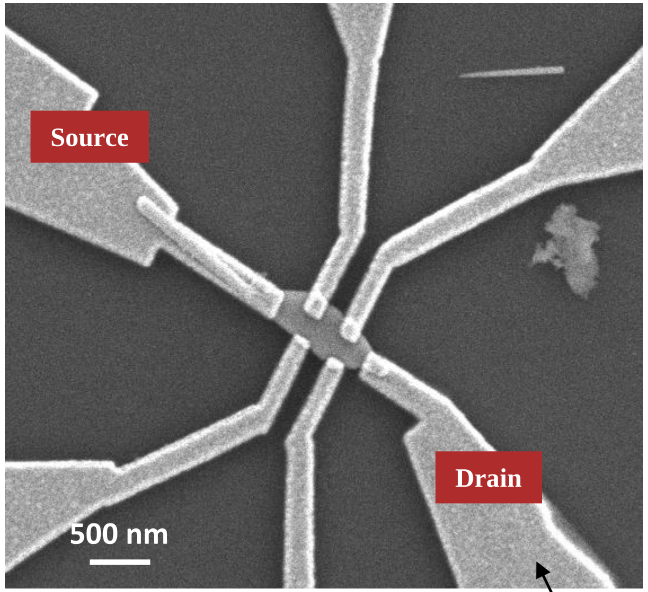
INSB NANOFLAGS: DEVICE FABRICATION AND TRANSPORT MEASUREMENTS



Ti/Au contacts

- ➢ InSb NFs are mechanically transferred to Si substrate
- ➢ Fabrication is done by electron beam lithography (EBL)followed by evaporation of Ti/Au for the contacts

INSB NANOFLAGS: DEVICE FABRICATION AND TRANSPORT MEASUREMENTS



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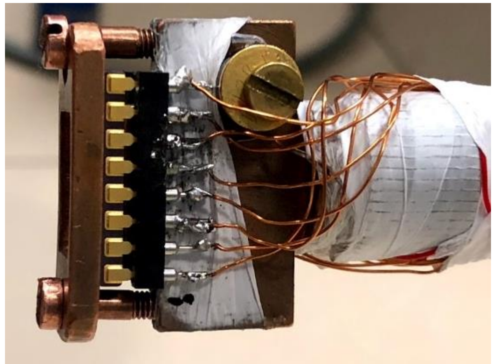
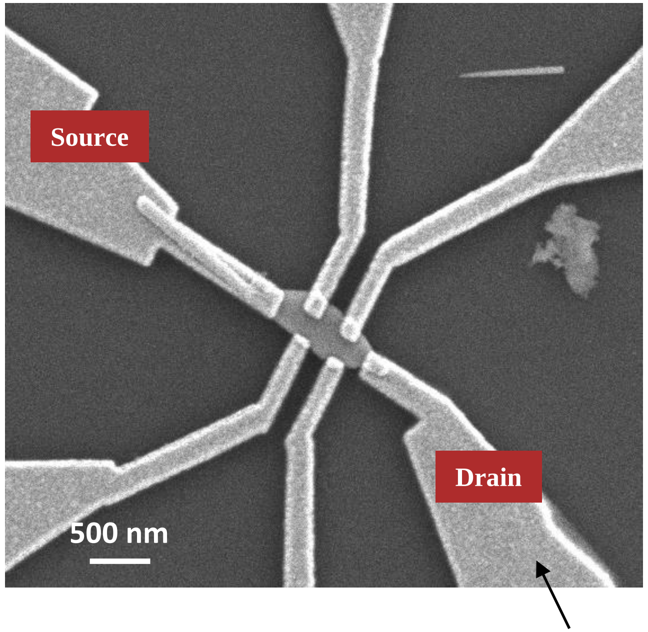


- InSb NFs are mechanically transferred to Si substrate
- Fabrication is done by electron beam lithography (EBL)followed by evaporation of Ti/Au for the contacts
- The Si substrate is pasted to the dual in line and contacts are bonded

InSb NANOFLAGS: DEVICE FABRICATION AND TRANSPORT MEASUREMENTS



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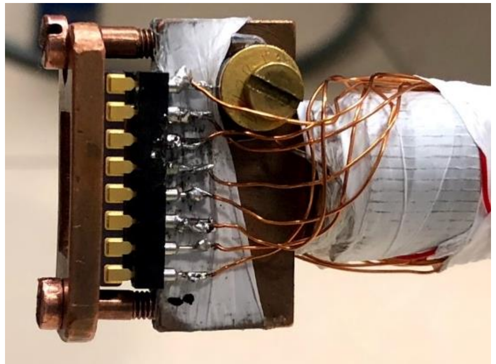
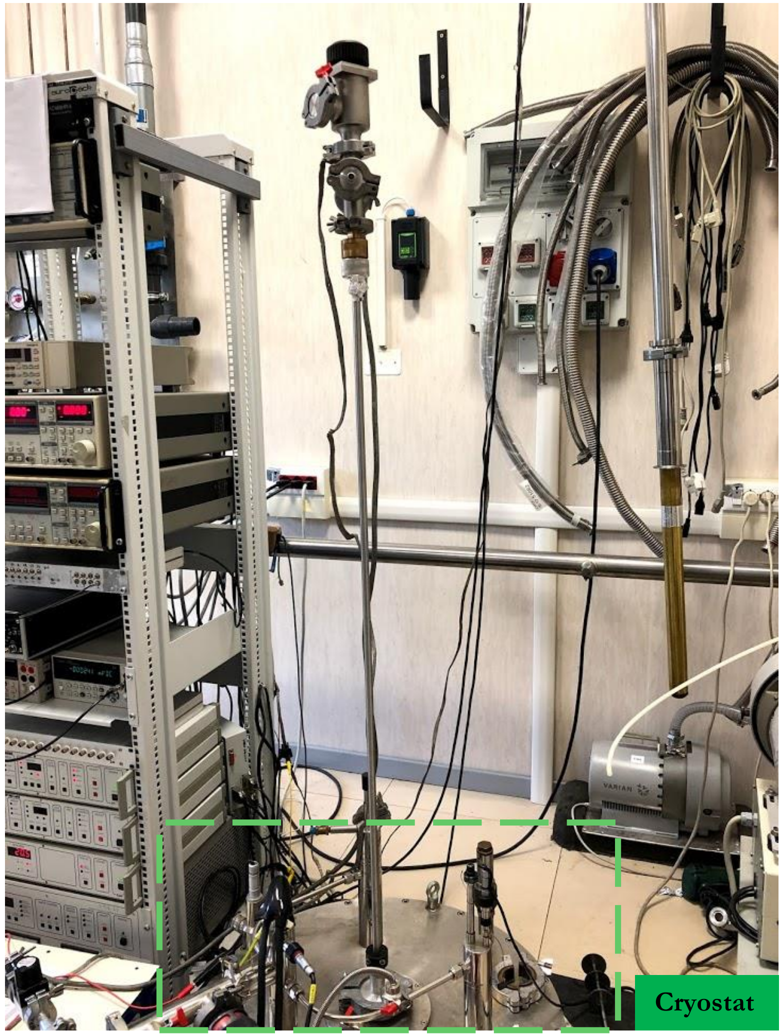
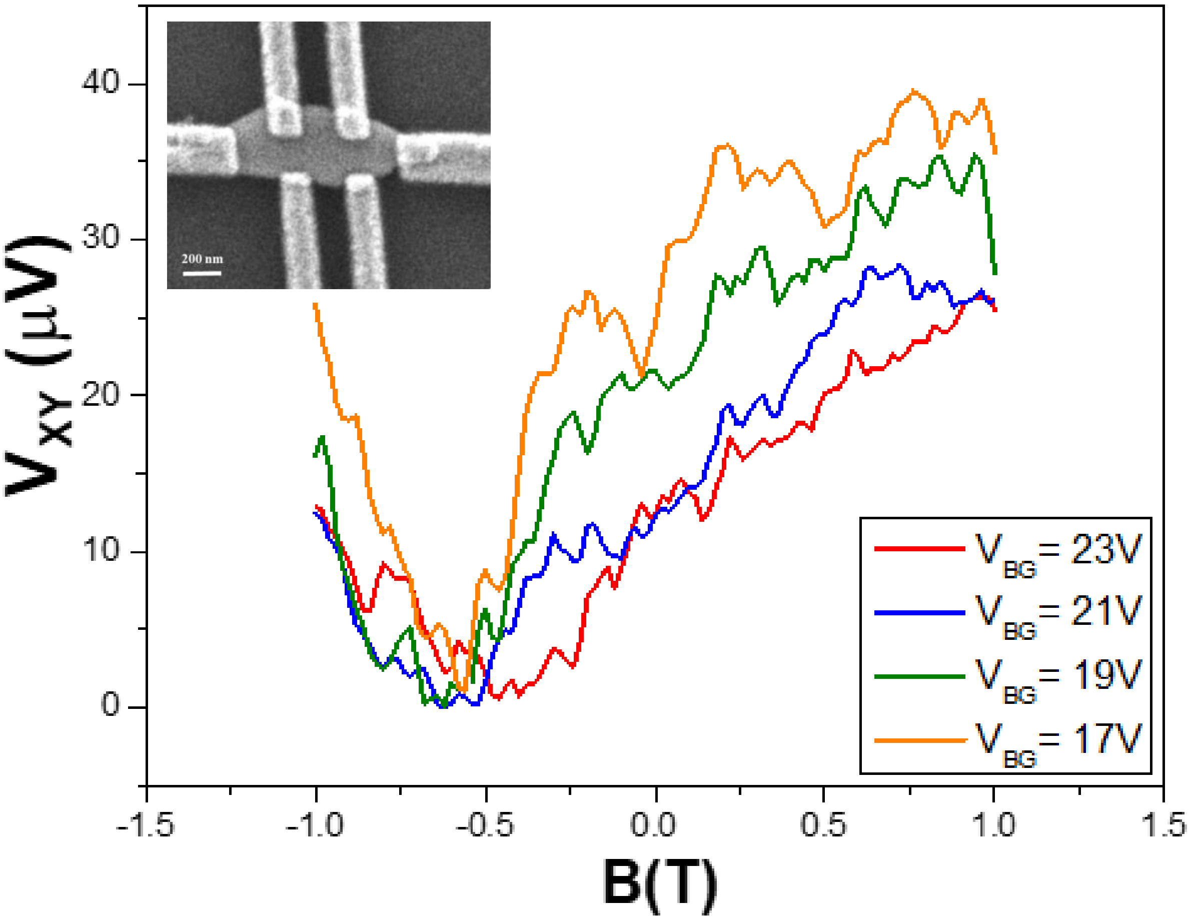
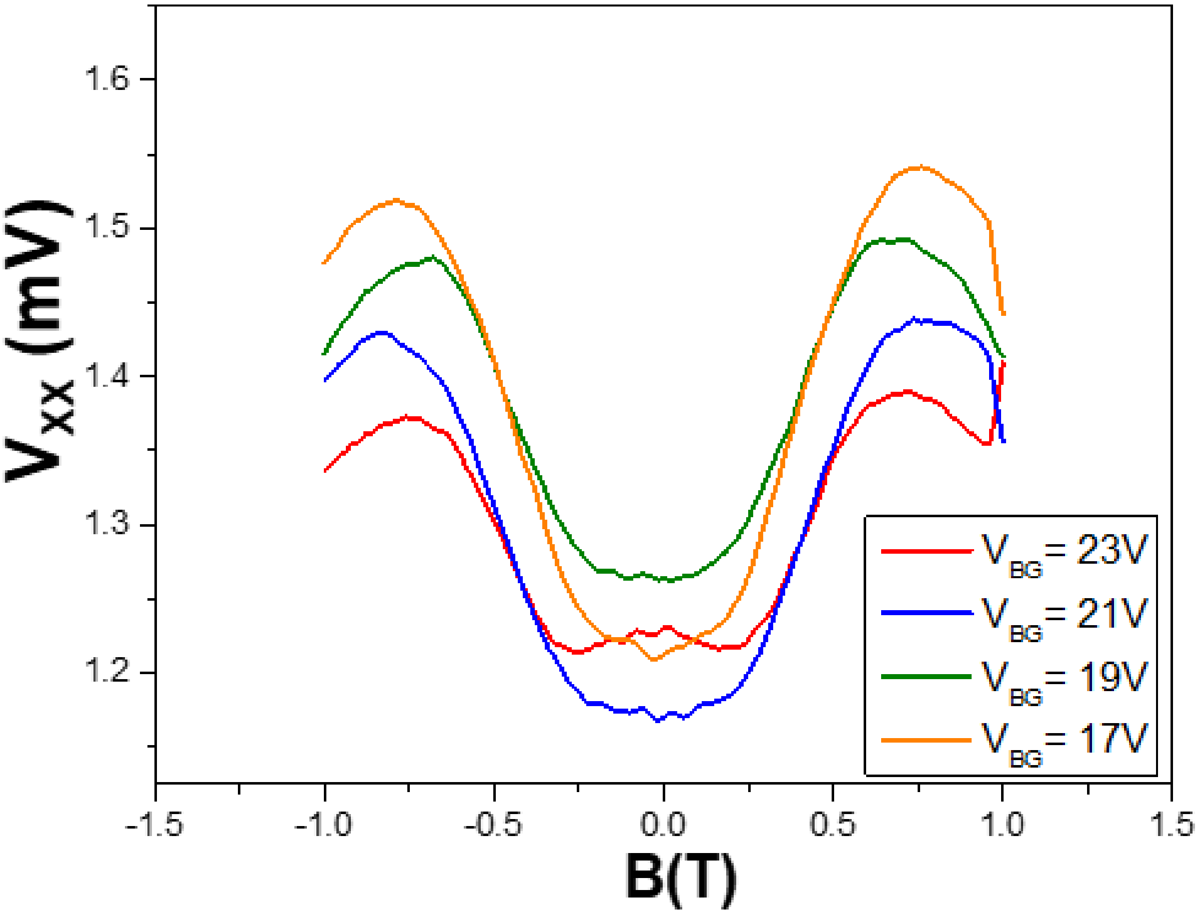




- InSb NFs are mechanically transferred to Si substrate
- Fabrication is done by electron beam lithography (EBL)followed by evaporation of Ti/Au for the contacts
- The Si substrate is pasted to the dual in line and contacts are bonded
- Transport measurements are performed in cryostat at liquid He temperature (4.2 K)

InSb NANOFLAGS: HALL MEASUREMENTS AT 4.2 K





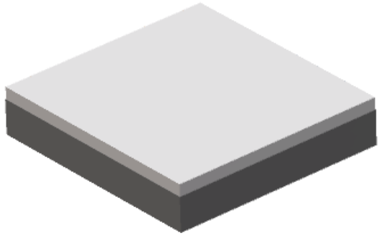
There is a mixing of the V_{XX} and V_{XY} components due to the reduced size of the NF, and hence correct value of electron carrier and mobility cannot be determined.

GROWTH APPROACH II
SELECTIVE AREA EPITAXY (SAE)

GROWTH APPROACH II: SELECTIVE AREA EPITAXY (SAE)

Sputtering

☐ SiO_2 ■ InSb



STEP 1

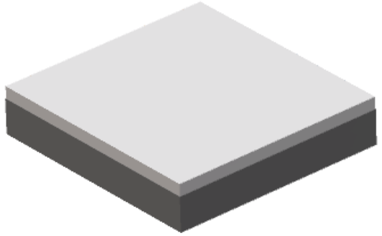
- Choosing the substrate.
- Deposition of 30 nm SiO_2 which acts as a mask.

The choice of substrate is
InSb (111) B
&
30 nm sputtered SiO_2 is
chosen to be the mask

GROWTH APPROACH II: SELECTIVE AREA EPITAXY (SAE)

Sputtering

⬜ SiO_2 ⬛ InSb



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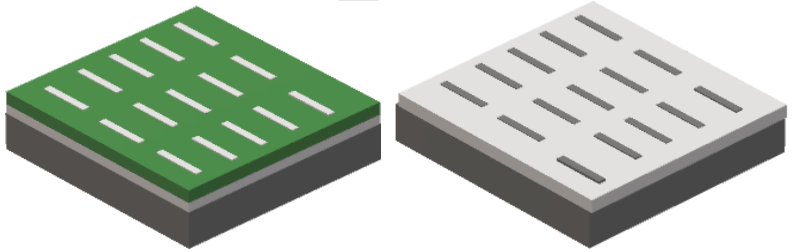
Patterning by EBL

🟩 CSAR

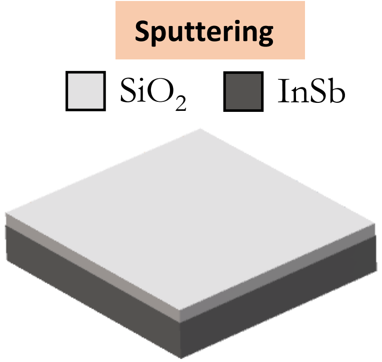


STEP 2

- Patterning slits of controlled thickness (55-100 nm) in preferential growth direction (Dose optimization, Development time, SiO_2 etching).

The choice of substrate is InSb (111) B & 30 nm sputtered SiO_2 is chosen to be the mask

GROWTH APPROACH II: SELECTIVE AREA EPITAXY (SAE)



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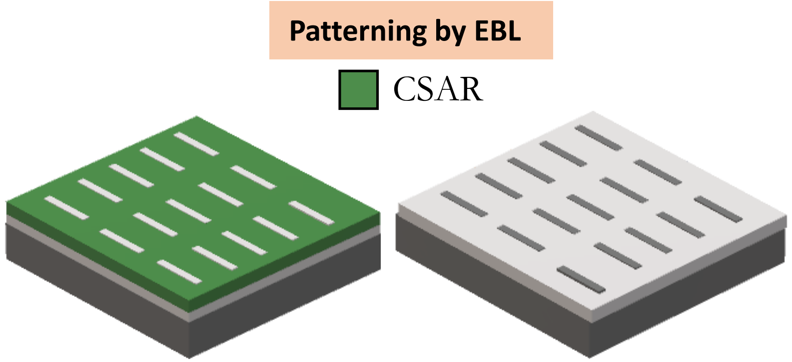

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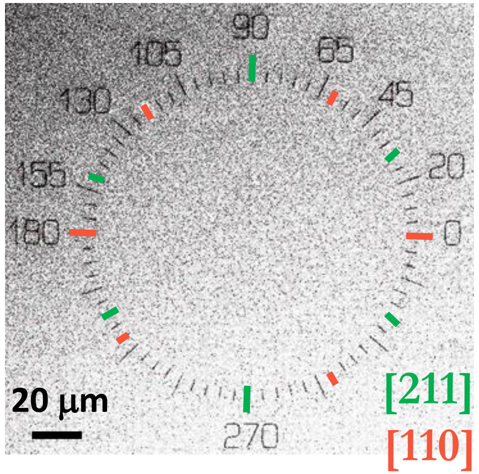
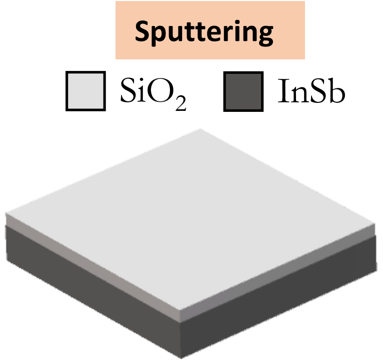


InSb segments grown along [211] and [110] directions are well faceted.

GROWTH APPROACH II: SELECTIVE AREA EPITAXY (SAE)



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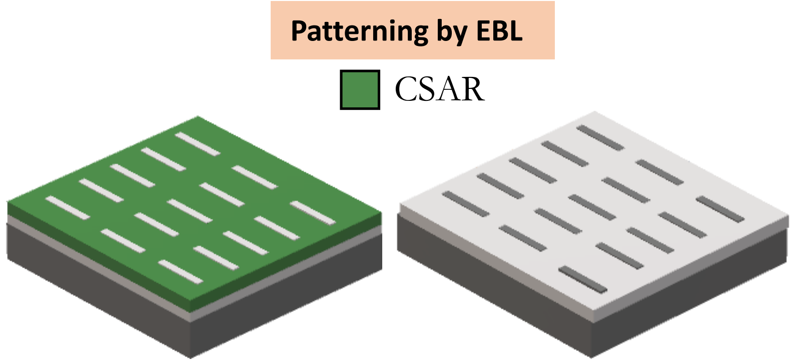

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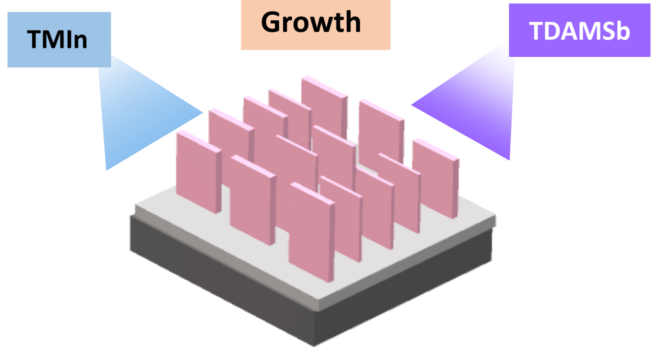


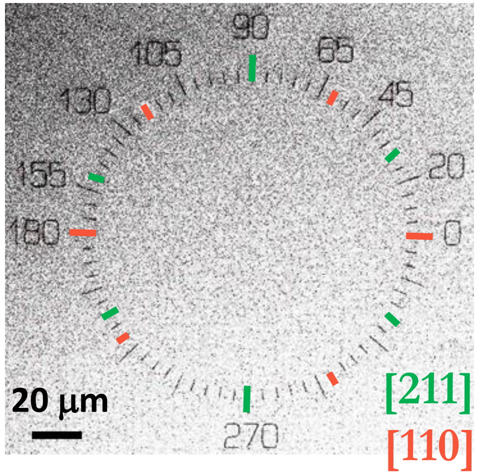
STEP 3

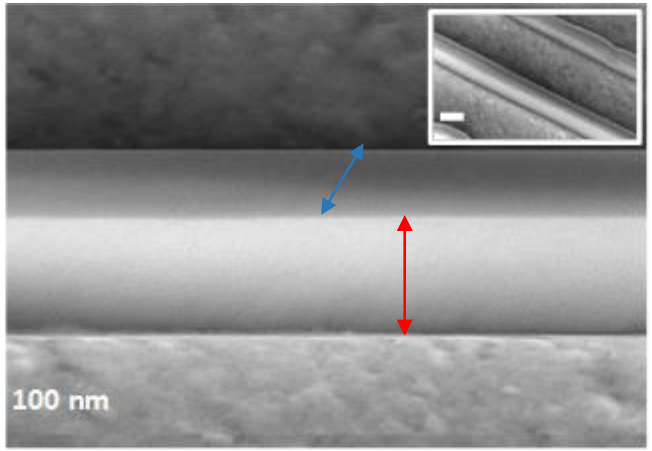
- Optimizing growth conditions for achieving large InSb flakes while having 50-100 nm thickness (growth temperature, fluxes, pitch, orientation).

The choice of substrate is InSb (111) B

&

30 nm sputtered SiO_2 is chosen to be the mask





Width= 110 nm

Height= 280 nm

FUTURE PLAN

- There's still some scope of improvement in diminishing the size of slit by optimizing etching step.

FUTURE PLAN

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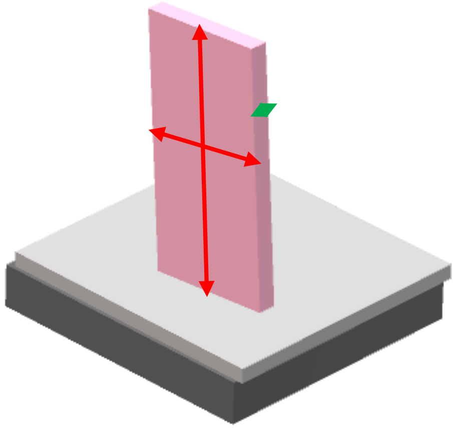
- After optimization of the above mentioned process, I have to optimize growth conditions in particular fluxes, growth temperature and inter slit distance such that the growth rate in axial direction is much greater than the growth rate in other directions. The targeted dimension of the flag is: lateral size >2 μm x 1 μm and thickness ~ 50nm.



FUTURE PLAN

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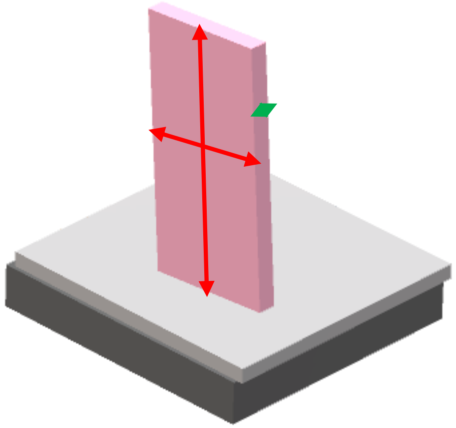
- After optimization of the above mentioned process, I have to optimize growth conditions in particular fluxes, growth temperature and inter slit distance such that the growth rate in axial direction is much greater than the growth rate in other directions. The targeted dimension of the flag is: lateral size >2 µm x 1 µm and thickness ~ 50nm.
- To fabricate the device and perform hall measurements on as grown InSb NFs from SAE.



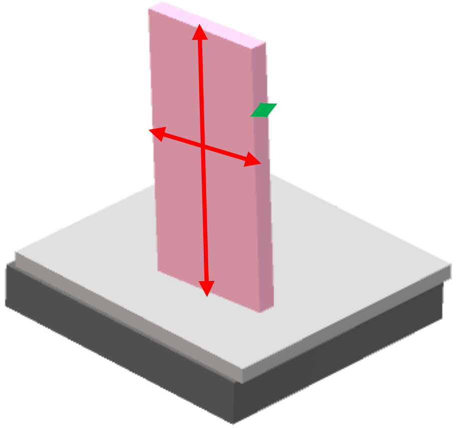
FUTURE PLAN

- There's still some scope of improvement in diminishing the size of slit by optimizing etching step.

- After optimization of the above mentioned process, I have to optimize growth conditions in particular fluxes, growth temperature and inter slit distance such that the growth rate in axial direction is much greater than the growth rate in other directions. The targeted dimension of the flag is: lateral size >2 µm x 1 µm and thickness ~ 50nm.

- To fabricate the device and perform hall measurements on as grown InSb NFs from SAE.

- In collaboration with Prof. Szabolcs Csonka group in Budapest University of Technology and Engineering, we are going to define 1D NW by electrostatic confinement potential of thin local gates below the flake and an ex-situ SC will be deposited between the wires (Project SuperTOP).



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Thank you for your attention